User's Guide
SLVU219–August 2007

Using the TPS40140EVM-003 A 32A Single Output Two Phase Stackable Synchronous Buck Converter

The TPS40140EVM-003 evaluation module (EVM) is a single output two phase synchronous buck converter. The EVM delivers 1.5V at 32A. The module uses the TPS40140 dual or 2-phase stackable synchronous buck controller. The EVM is also stackable with the other EVM to construct a multiphase converter.

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1 Description

TPS40140EVM-003 is designed to use a regulated 10.8V to 13.2V bus to produce high-current regulated output. The TPS40140EVM-003 evaluation module demonstrates the TPS40140 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40140 in a given application.

1.1 Applications

- Graphics Cards
- Internet Servers
- Networking Equipment
- Telecommunications Equipment
- DC Power Distributed Systems

1.2 Features

- 10.8 V–13.2 V input range
- 1.5 V fixed output
- 32 Adc Steady State Current per Output
- 500 kHz switching frequency per Phase
- Single Main Switch N-channel MOSFET and Two Synchronous Rectifier N-channel MOSFETs per phase
- Convenient test points for probing critical waveforms and non-invasive loop response testing

2 TPS40140EVM-003 Electrical Performance Specifications

Table 1. TPS40140EVM-003 Electrical and Performance Specifications

Parameter	Notes and Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range		10.8		13.2	V
Max Input Current	V_{IN} = 10.8 V, I_{OUT} = 32 A		5.1		A
No-Load Input Current	V_{IN} = 13.2 V, I_{OUT} = 0 A		130		mA
OUTPUT CHARACTERISTICS					
OUTPUT (V_{OUT})					
Output Voltage			1.51		V
Output Voltage Regulation	Line Regulation (10.8 V <V_{IN} <13.2 V, I_{OUT} = 10 A)			0.1%	
	Load Regulation (0A <I_{OUT} <32 A, V_{IN} = 12 V)			0.5%	
Output Voltage Ripple	V_{IN} = 13.2 V, I_{OUT} = 32 A		15		mVpp
Output Load Current	I_{OUT}	0		32	A
Output Over Current				40	A
SYSTEM CHARACTERISTICS					
Switching Frequency			500		kHz
Peak Efficiency	V_{OUT} = 1.5 V, I_{OUT} = 20 A, V_{IN} = 10.8 V		87.5%		
Full Load Efficiency	V_{OUT} = 1.5 V, I_{OUT} = 32 A, V_{IN} = 12 V		86.8%		

3 Schematic

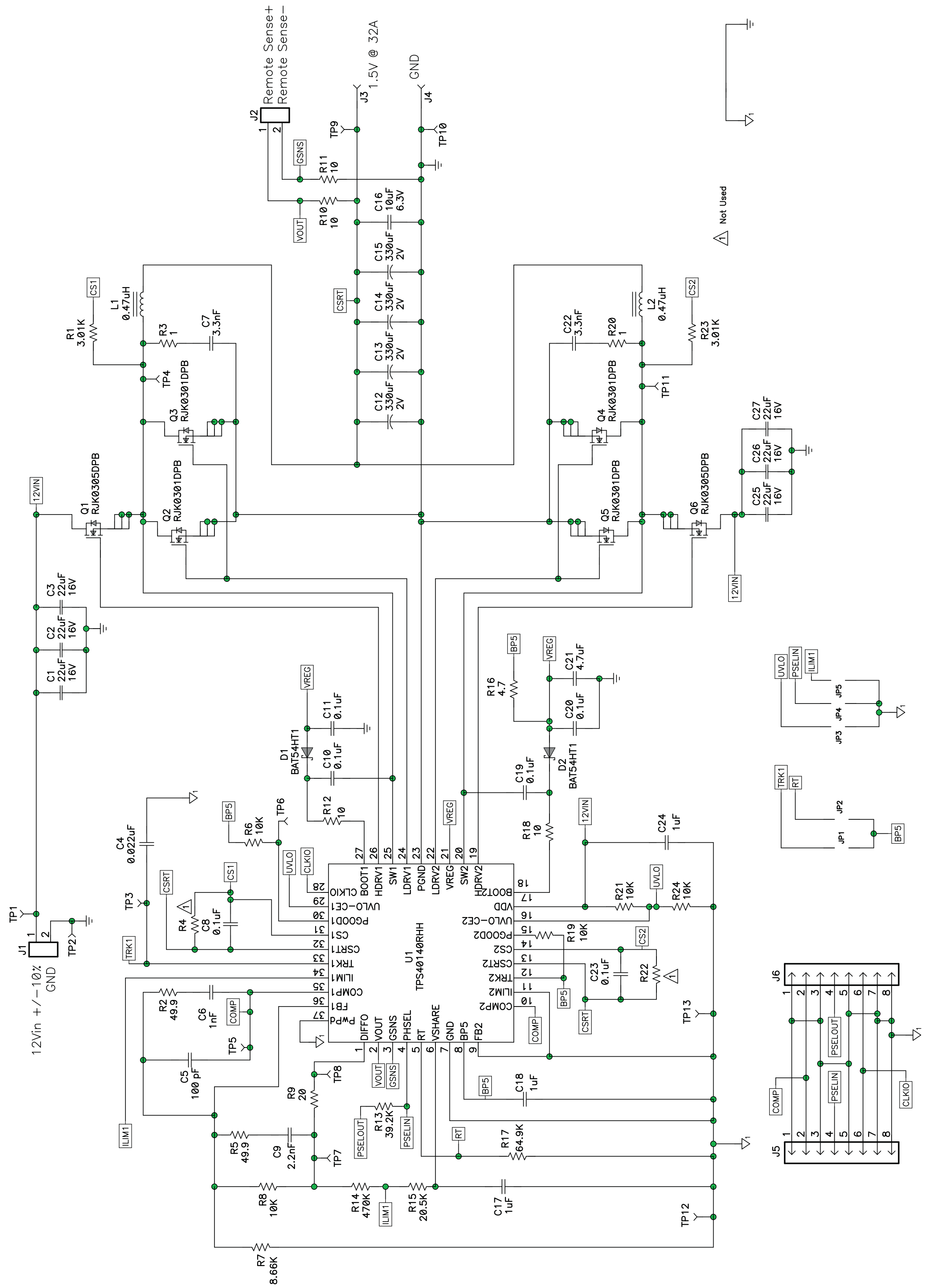


Figure 1. TPS40140EVM-003 Schematic
For Reference Only, See Table 3: Bill of Materials for Specific Values

4 Test Set Up

4.1 Recommended Test Equipment

4.1.1 Voltage Source

V_{IN}
The input voltage source (V_{IN}) should be a 0–15V variable DC source capable of 10 Adc. Connect VIN to J1 as shown in Figure 2.

4.1.2 Meters

V1: V_{IN}, 0–15V voltmeter
V2: V_{OUT}, 0–5V voltmeter
I1: 0–10A current meter

4.1.3 Load

LOAD
The Output Load (LOAD) should be an Electronic Constant Current Mode Load capable of 0–40Adc at 1.5V

4.1.4 Oscilloscope

A Digital or Analog Oscilloscope can be used to measure the ripple voltage on V_{OUT}. The Oscilloscope should be set for 1MΩ impedance, 20MHz Bandwidth, AC coupling, 1μs/division horizontal resolution, 10mV/division vertical resolution for taking output ripple measurements. Test points TP9 and TP10 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP9 and holding the ground barrel to TP10 as shown in Figure 3. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

V_{IN} to J1
The connection between the source voltage, V_{IN} and J1 of the EVM can carry as much as 6 Amps DC. The minimum recommended wire size is 1x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J3, J4 to LOAD (Power)
The power connection between J3 and J4 of the EVM and LOAD can carry as much as 32Adc. The minimum recommended wire size is 2x AWG #14, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

4.1.6 Other

FAN
This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS40140EVM-003.

Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.

4.2.1 Input Connections

1. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from VIN to 6A maximum. Make sure V_{IN} is initially set to 0V and connected as shown in Figure 2.

4.2.2 Output Connections

1. Connect LOAD to J3 and J4, set LOAD to constant current mode to sink 0 Adc before V_{IN} is applied.
2. Connect voltmeter, V2, across TP9 and TP10, as shown in Figure 2.

4.2.3 Other Connections

1. Place Fan as shown in Figure 2 and turn on, making sure air is flowing across the EVM.

4.2.4 Set Up Diagram

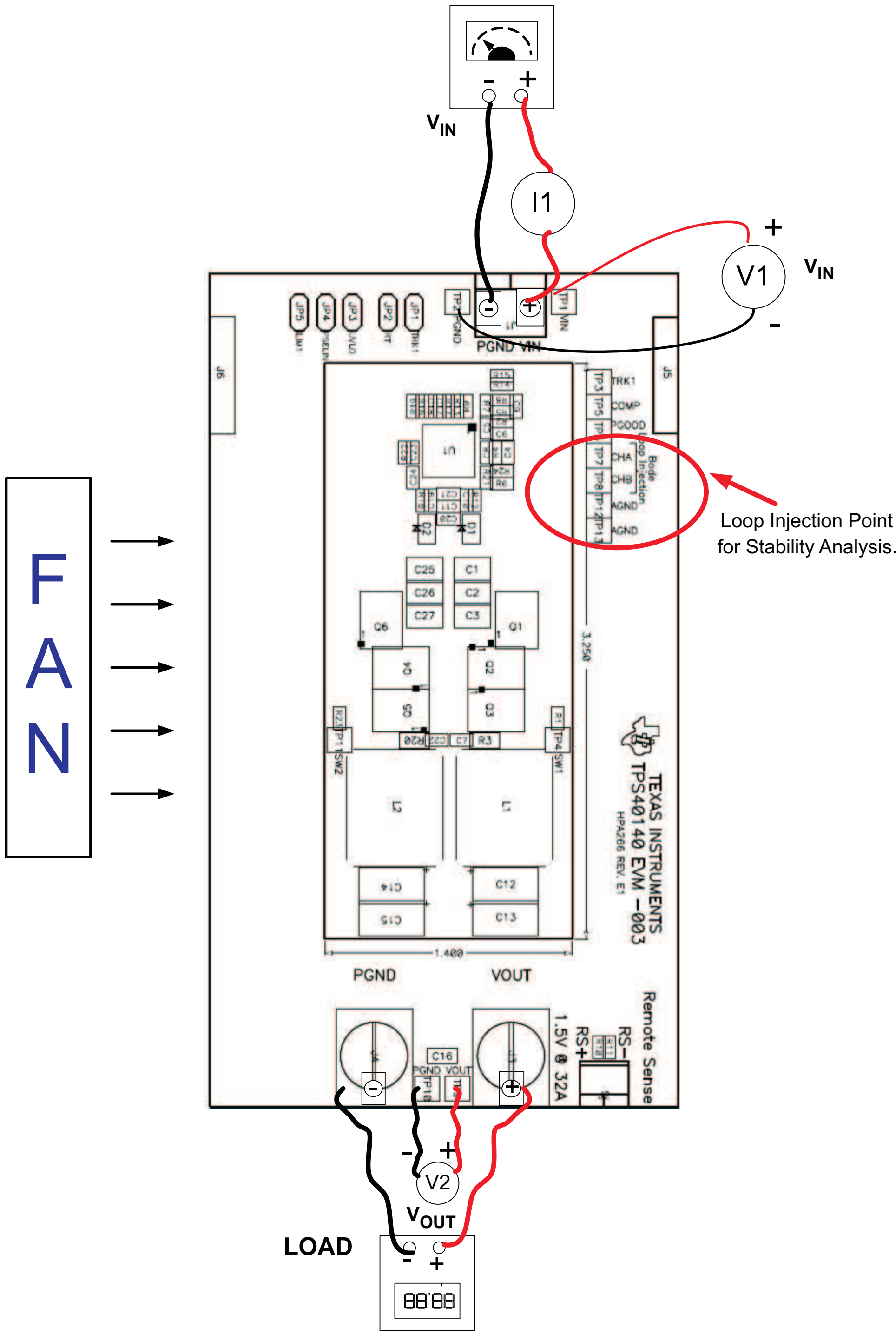
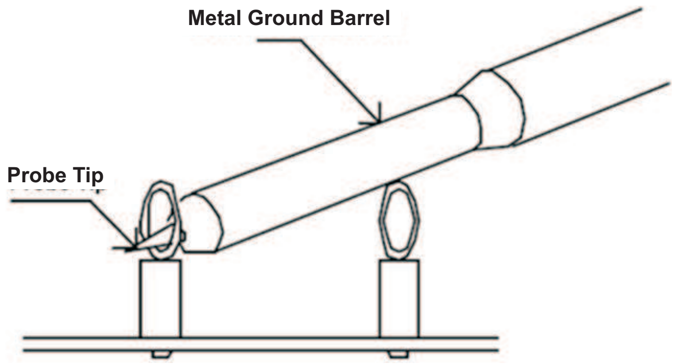


Figure 2. TPS40140EVM-003 Recommended Test Set-Up



Tip and Barrel Output Ripple Measurement

Figure 3. Output Ripple Measurement

4.3 Start Up and Test Procedure

1. Ensure LOAD is set to constant current mode and to sink 0 Adc.
2. Increase V_{IN} from 0 V to 10.8 Vdc, V_{OUT} should be in regulation per Table 1. Continue increasing V_{IN} to 12 V.
3. Vary LOAD from 0 to 32 Adc, V_{OUT} should remain in regulation per Table 1.
4. Vary V_{IN} from 10.8 Vdc to 13.2 Vdc, V_{OUT} should remain in regulation per Table 1.
5. For various V_{IN} settings vary LOAD from 0 to 32 Adc. V_{OUT} should remain in regulation per Table 1 for all combinations of load on LOAD up to 32 A.

4.4 Control Loop Gain and Phase Measurement Procedure

1. Connect 1 kHz–1 MHz Isolation Transformer to test points marked CHA and CHB.
2. Connect Input Signal Amplitude Measurement Probe (Channel A) to CHA.
3. Connect Output Signal Amplitude Measurement Probe (Channel B) to CHB.
4. Connect Ground Lead of Channel A and Channel B to AGND
5. Inject 25 mV or less signal through the Isolation Transformer.
6. Sweep Frequency from 100 Hz to 1 MHz with 10 Hz or lower post filter.
7. Control Loop Gain can be measured by $20 \times LOG\left(\frac{ChannelB}{ChannelA}\right)$
8. Control Loop Phase is measured by the Phase difference between Channel A and Channel B.
9. Disconnect Isolation Transformer from the bode plot test points before making other measurements (Signal Injection into Feedback may interfere with accuracy of other measurements).

4.5 EVM Configuration

4.5.1 Two Phase Single Output Configuration (Default)

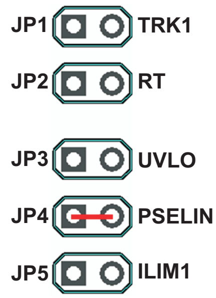


Figure 4. Default Configuration

JP4 is shorted with a jumper and others are left open. In this configuration, the EVM operates as a two phase single output converter.

4.5.2 Disabling the Output

JP3 allows the user to disable or enable the output. The output is disabled by shorting JP3 with a Jumper.

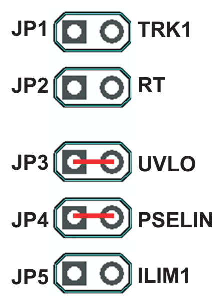


Figure 5. Output Disable Configuration

4.5.3 Multiphase Configuration

This EVM is stackable with other identical boards. For example, two EVMs can construct a fully interleaved four phase converter. In Figure 6, the EVM is configured as a master while stacking with the other EVM board.

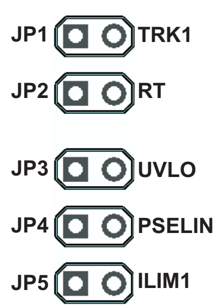


Figure 6. Configure the EVM as a Master for Stackable Operation

If two EVM boards are stacked together, the other EVM is configured as a slave as shown in Figure 7.

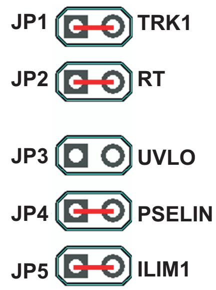


Figure 7. Configure the EVM as a Slave for Stackable Operation

If more than two EVM boards are stacked, for example three, the two slave EVMs have slightly different settings. Considering the master is the first board in the chain and all others are slaves, JP4 in the last slave board should be shorted by a jumper while it is left as open in other slave boards. The configurations are shown in Figure 8.

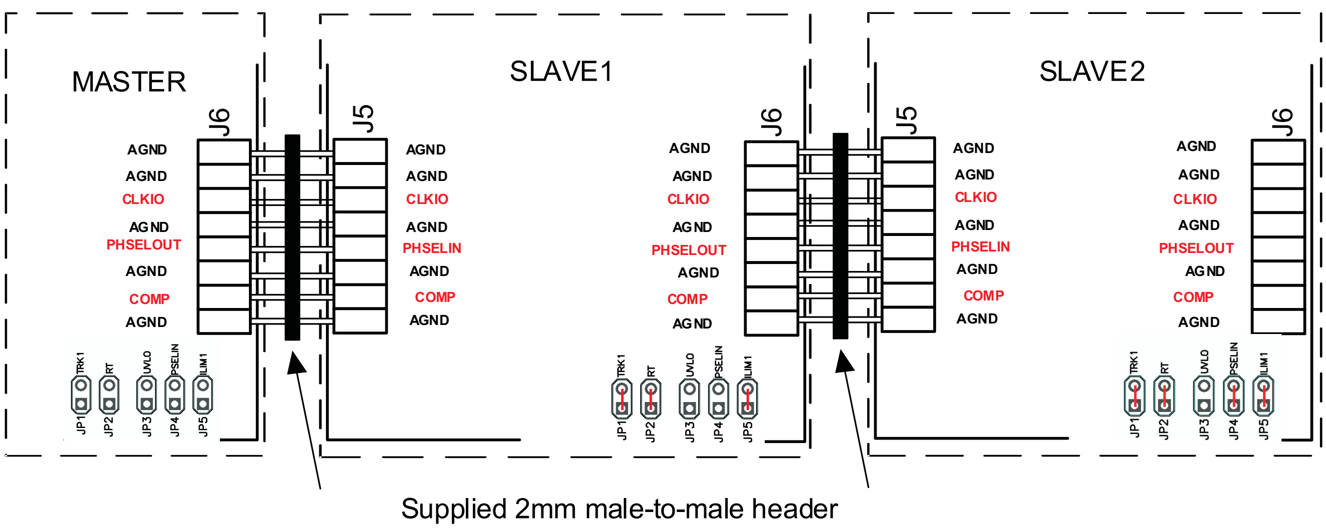


Figure 8. Master and Slave Connection (this EVM is the slave)

J5 and J6 are used to connect the EVM to the other EVM boards. Male-to-male headers are provided to make the connections between the boards.

4.6 Test Points

Several test points are located around the board. These can be used to sense what is occurring at different points of the converter. Table 2 lists these test points and what they are used for.

Table 2. List of Test Points

NAME	TEST POINT LABEL	DESCRIPTION
TP1	VIN	Input voltage positive sense point
TP2	PGND	Input voltage negative sense point
TP3	TRK1	Soft Start
TP4	SW1	Channel 1 switch node
TP5	COMP	Error amplifier output
TP6	PGOOD	Power Good
TP7	CHA	Loop injection point CHA
TP8	CHB	Loop injection point CHB
TP9	VOUT	Output positive sense point
TP10	PGND	Output negative sense point
TP11	SW2	Channel 2 switch node
TP12	AGND	Analog Ground
TP13	AGND	Analog Ground

4.7 Equipment Shutdown

1. Shut down LOAD
2. Shut down V_{IN}
3. Shut down FAN

5 TPS40140EVM-003 Typical Performance Data and Characteristic Curves

Figure 9 through Figure 13 present typical performance curves for the TPS40140EVM-003. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

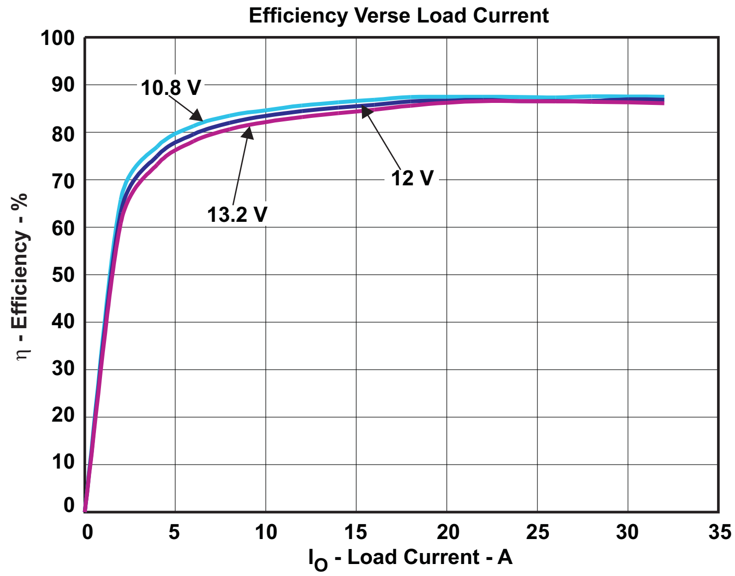


Figure 9. TPS40140EVM-003 Efficiency
V_{IN} = 10.8–13.2 V, V_{OUT} = 1.5 V, I_{OUT} = 0–32A

5.2 Line and Load Regulation

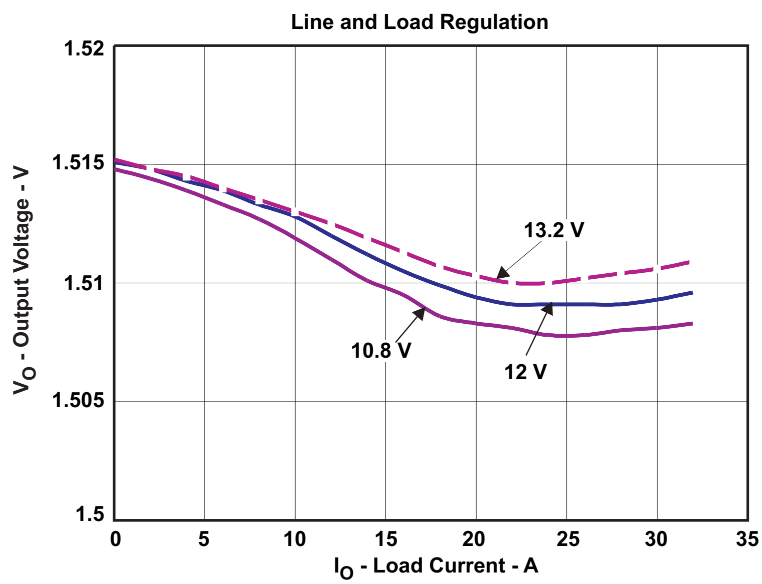


Figure 10. TPS40140EVM-003 V_{OUT} = 1.5V Load Regulation

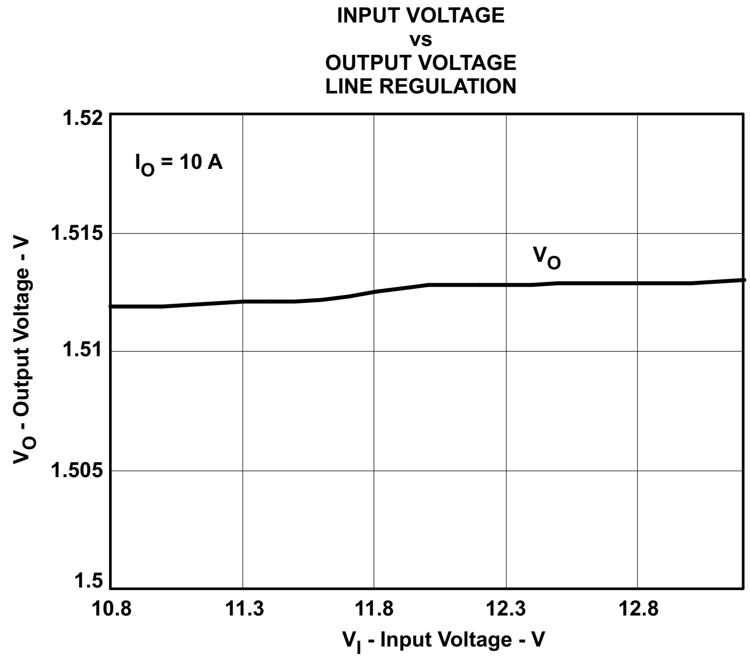


Figure 11. TPS40140EVM-003 V_{OUT} = 1.5V Line Regulation

5.3 Bode Plot

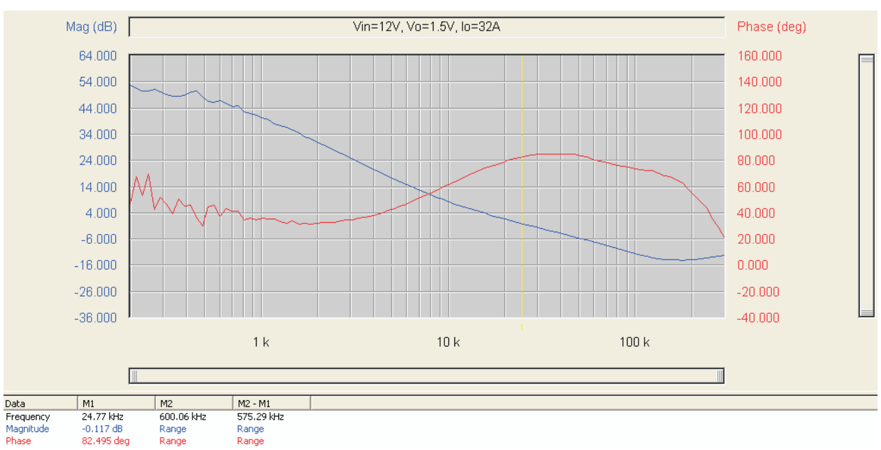


Figure 12. TPS40140EVM-003 Loop Gain, BW = 25 kHz, Phase Margin = 82°

5.4 Transient Response

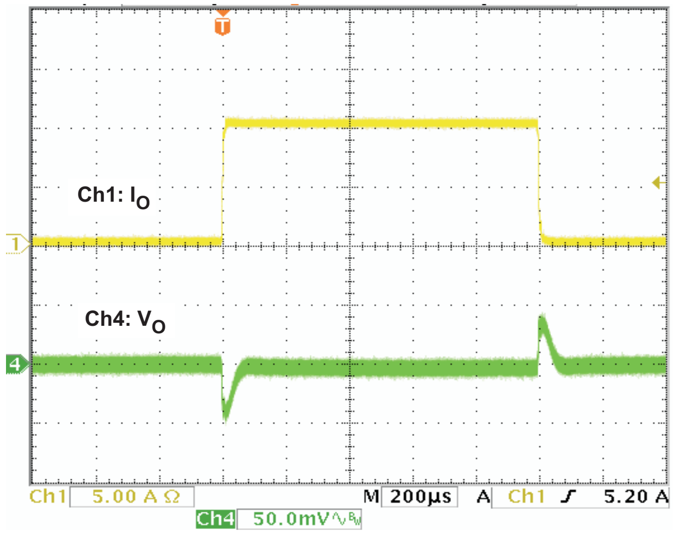


Figure 13. Transient Response 10 A Step, 2.5 A/µs, 50 mV/div
Ch1: Iout; Ch4: Vout

6 EVM Assembly Drawings and Layout

Figure 14 through Figure 18 show the design of the TPS40140EVM-003 printed circuit board. The EVM has been designed using a four layer, 2 oz copper-clad circuit board with all components on the top side to allow the user to easily view, probe and evaluate the TPS40140 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

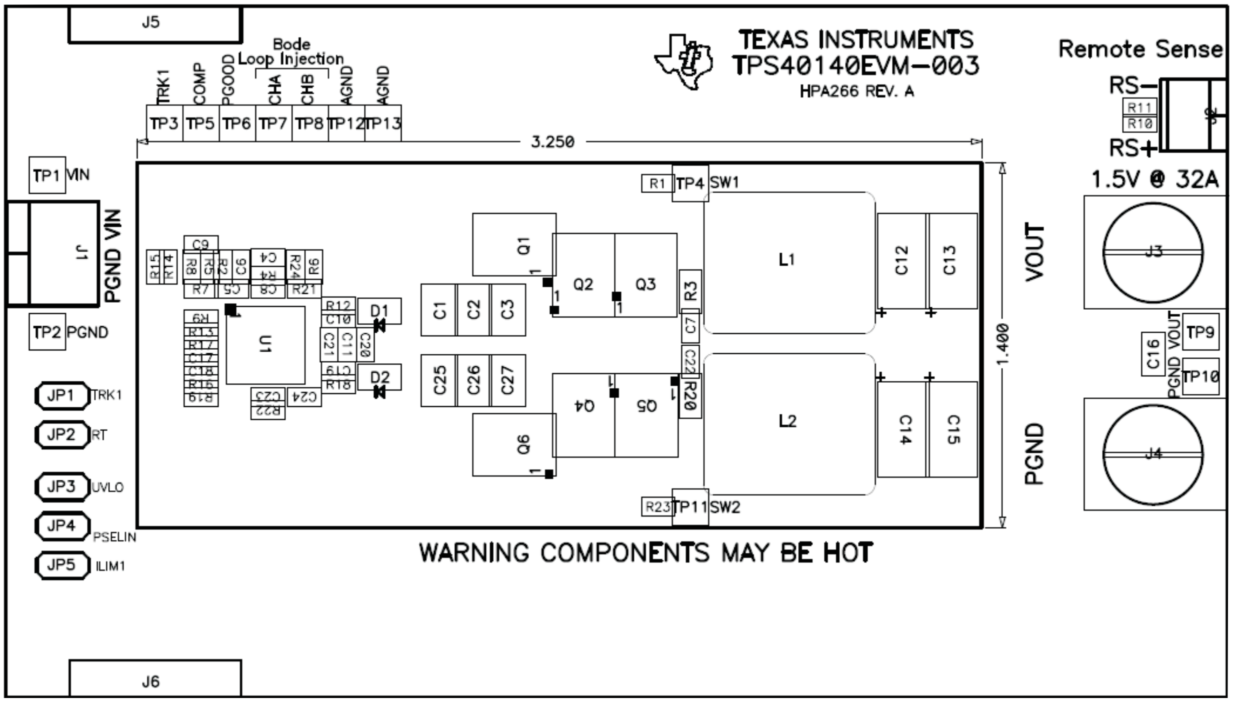


Figure 14. TPS40140EVM-003 Component Placement (Viewed from Top)

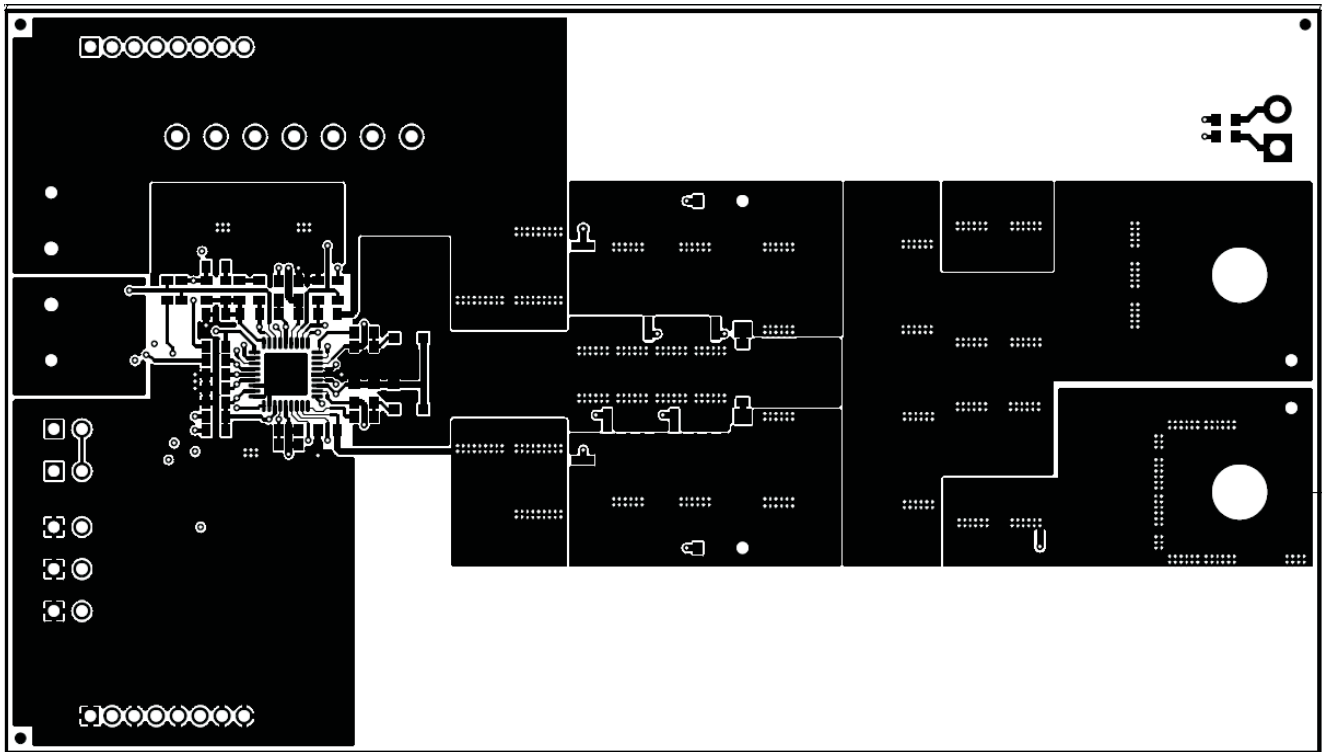


Figure 15. TPS40140EVM-003 Top Copper (Viewed from Top)

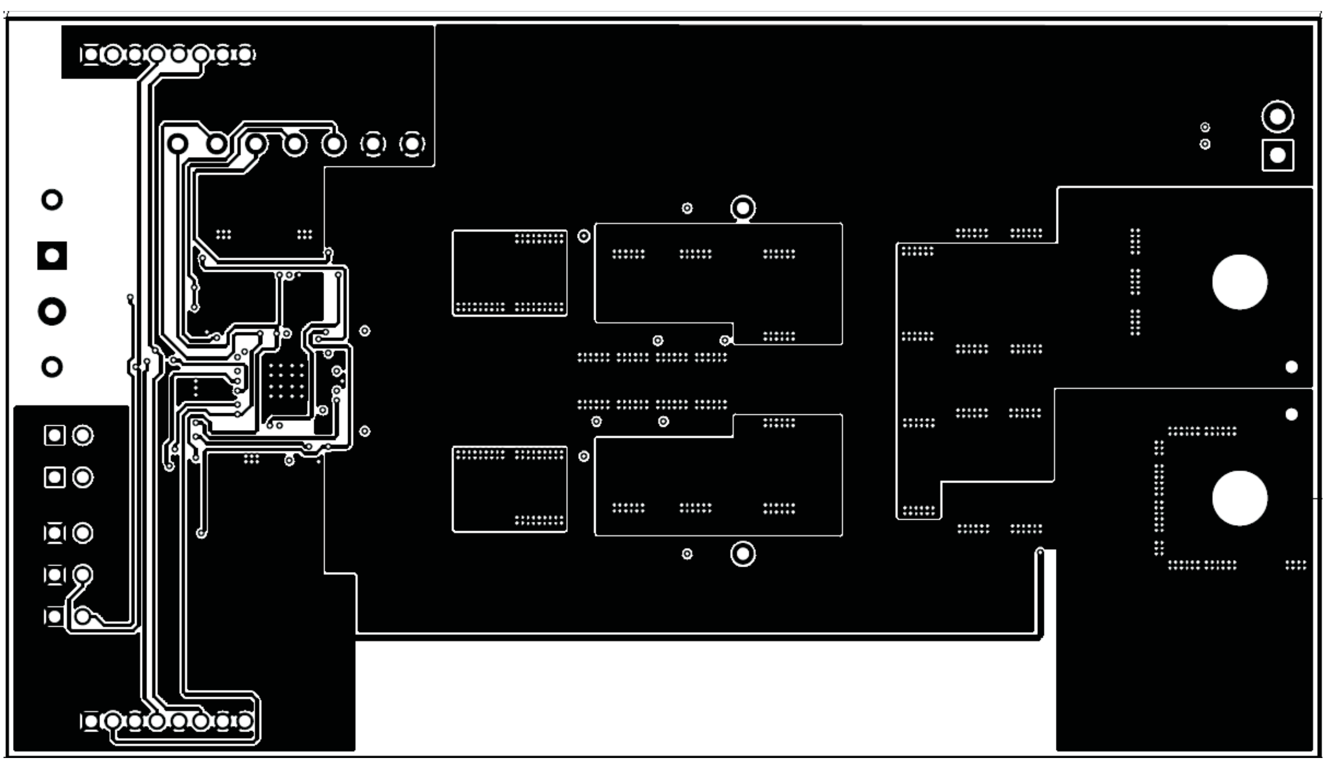


Figure 16. TPS40140EVM-003 Layer 2 Copper (X-Ray View from Top)

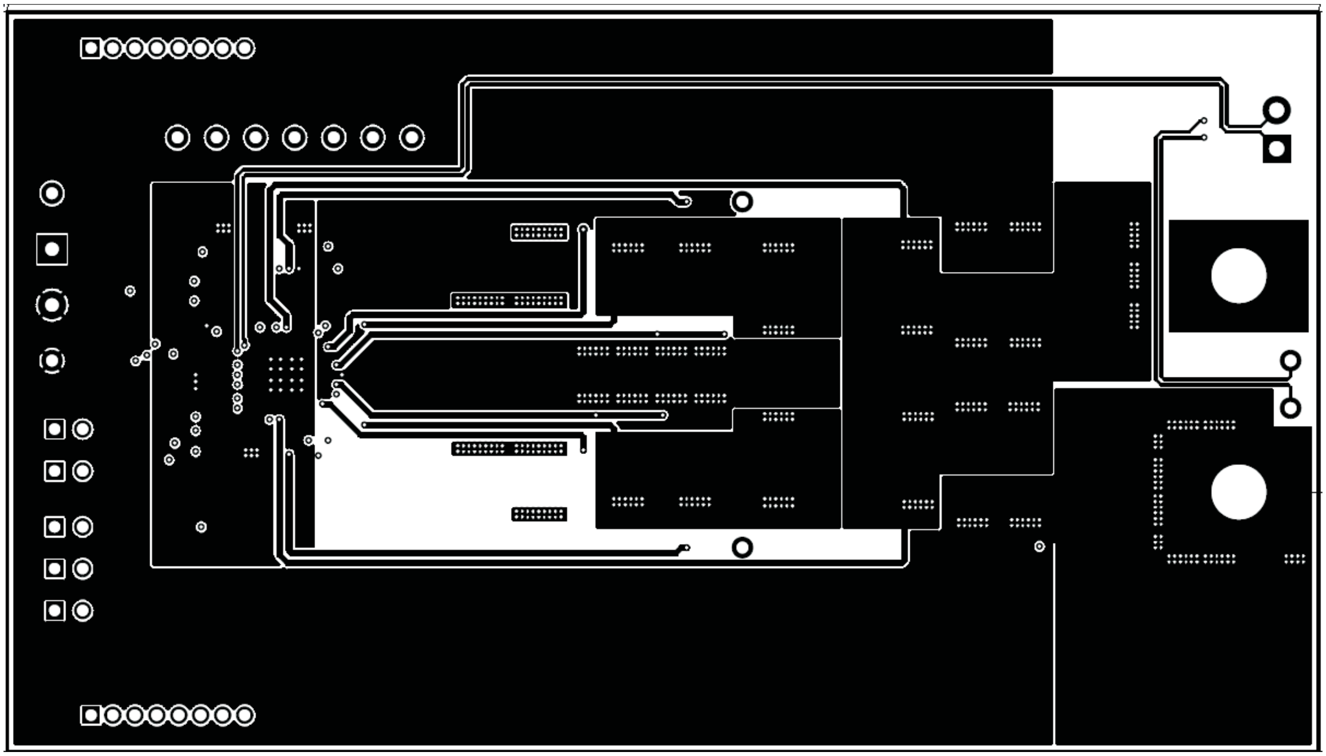


Figure 17. TPS40140EVM-003 Layer 3 Copper (X-Ray View from Top)

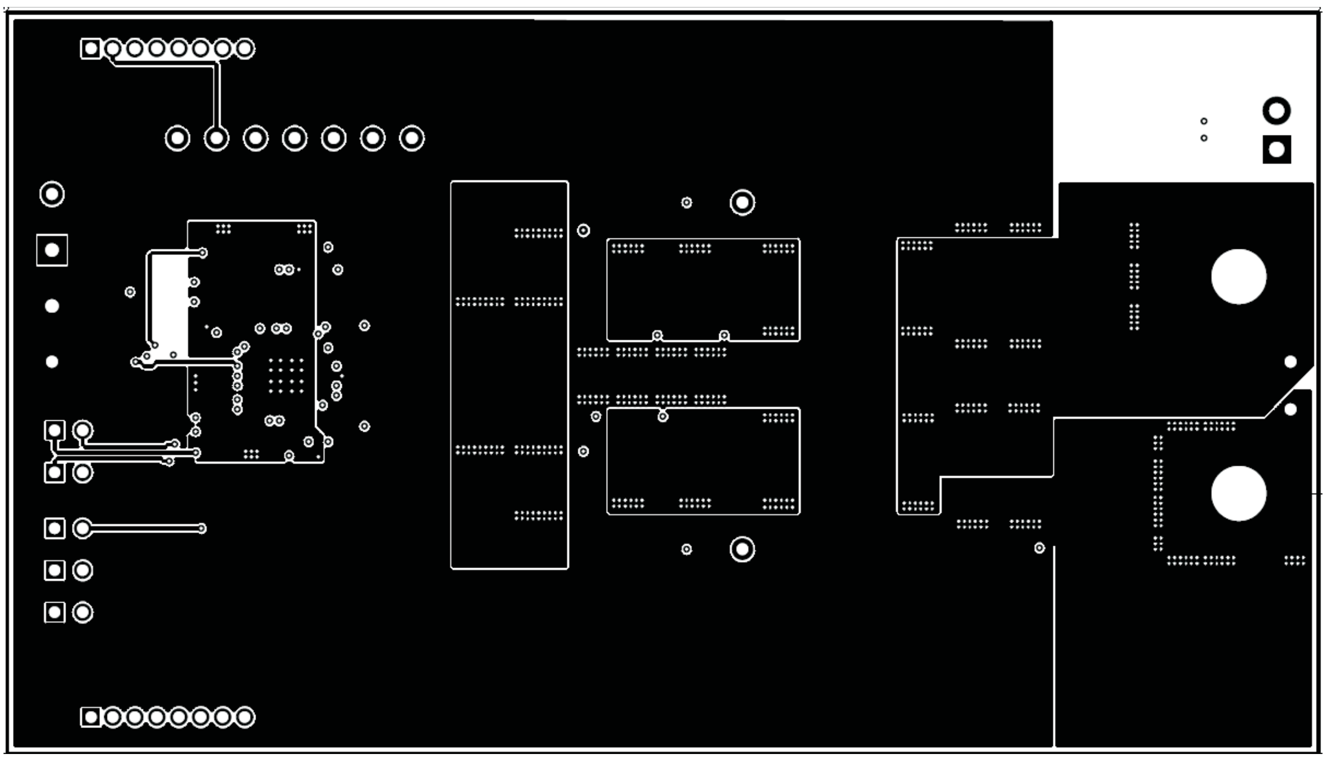


Figure 18. TPS40140EVM-003 Bottom Copper (X-Ray View from Top)

7 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS40140EVM-003 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
6	C1–C3, C25–C27	22 µF	Capacitor, Ceramic, 16V, X5R, 20%	1210	Std	Std
4	C12–C15	330uF	Capacitor, SP-Cap, 2V, 0.006 Ω, 20%	7343	EEFSX0D331XE	Panasonic
1	C16	10 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	805	Std	Std
3	C17, C18, C24	1 µF	Capacitor, Ceramic, 16V, X5R, 10%	603	Std	Std
1	C21	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	603	Std	Std
1	C4	22 nF	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
1	C5	100 pF	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
1	C6	1000 pF	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
2	C7, C22	3.3 nF	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
6	C8, C10, C11, C19, C20, C23	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
1	C9	2.2 nF	Capacitor, Ceramic, 16V, X7R, 10%	603	Std	Std
2	D1, D2	BAT54HT1	Diode, Schottky, 30V, 0.35Vf	SOD323	BAT54HT1	On Semi
1	J1	ED1609	Terminal Block, 2-pin, 15-A, 5,1mm	0.40 × 0.35 in	ED1609	OST
1	J2	ED1514	Terminal Block, 2-pin, 6-A, 3,5mm	0.27 × 0.25 in	ED1514	OST
2	J3, J4	524600	Lug, Solderless, #2 - #8 AWG, 1/4	1.55 × 0.50 in	524600	ILSCO
2	J5, J6	PPPN081FGGN	Conn,recept, 2mm, 8-pin Right Angle, Female (36-pin Strip)	0.079 × 8 in	PPPN081FGGN	Sullins
5	JP1–JP5	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 in × 2	PTC36SAAN	Sullins
2	L1, L2	0.47 µH	Inductor, SMT, 41A, 0.001Ω	0.512 × 0.571 in	IHLP-5050FD-0R47-M01	Vishay
2	Q1, Q6	RJK0305	MOSFET, N-Ch, 30V, 15A, 0.013Ω, LFPAK	LFPAK	RJK0305DPB	Renesas
4	Q2–Q5	RJK0301	MOSFET, N-Ch, 30V, 30A, 0.004Ω, LFPAK	LFPAK	RJK0301DPB	Renesas
2	R1, R23	3.01K	Resistor, Chip, 1/16W,1%	603	Std	Std
4	R10–R12, R18	10.0	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R16	4.70	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R14	470K	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R15	20.5K	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R17	64.9K	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R13	39.2K	Resistor, Chip, 1/16W, 1%	603	Std	Std
2	R3, R20	1.00	Resistor, Chip, 1/8W, 1%	805	Std	Std
1	R9	20.0	Resistor, Chip, 1/16W, 1%	603	Std	Std
0	R4, R22	OPEN	Resistor, Chip, 1/16W, 1%	603	Std	Std
2	R2,R5	49.9	Resistor, Chip, 1/16W, 1%	603	Std	Std

Table 3. TPS40140EVM-003 Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR
5	R6, R8, R19, R21, R24	10.0K	Resistor, Chip, 1/16W, 1%	603	Std	Std
1	R7	8.66K	Resistor, Chip, 1/16W, 1%	603	Std	Std
2	TP1, TP9	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 in	5000	Keystone
4	TP2, TP10, TP12, TP13	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 in	5001	Keystone
7	TP3–TP8, TP11	5002	Test Point, White, Thru Hole Color Keyed	0.100 × 0.100 in	5002	Keystone
1	U1	TPS40140RHH	IC, 2-Phase or Dual Output PWM Controller, QFN	QFN-36	TPS40140RHH	Texas Instruments

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10.8 V to 13.2 V and the output voltage range of 1.5 V at 0–32 A.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85 °C. The EVM is designed to operate properly with certain components above 85 °C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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